Yan Sun

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Education:

University of Illinois at Urbana-Champaign **Dec 2023—present**

- PhD. Candidate
- Advisor: Prof. Nam Sung Kim
- Rambus Computer Engineering Fellowship (2024-2025)

University of Illinois at Urbana-Champaign, GPA 3.85/4 **Jan 2022–Dec 2023**

- Master of Science in Electrical and Computer Engineering
- Advisor: Prof. Nam Sung Kim
- Best Demo Award (Fall 2023)
  - PRISM – JUMP 2.0 - Semiconductor Research Corporation (SRC) annual review.

University of Illinois at Urbana-Champaign, GPA 3.96/4 **Aug 2018–Dec 2021**

- B.S. in Computer Engineering, Minor in Statistic
- Highest Honor
- James Scholar in Engineering
- Dean's List (Top 20%): all semesters
- Undergraduate TA for ECE411 (Introduction to Computer Architecture)

Experience:

Meta Platforms (Menlo Park, CA) **May 2025-Aug 2025**

- **Summer Research Internship**

Samsung Semiconductor (San Jose, CA) **May 2024-Aug 2024**

- **Summer Research Internship**
  - Worked as an intern in the memory solution lab (MSL) and researched about CXL memory pool.
  - **Manager**: Changho Choi
  - **Mentor**: Heekwon Park

Samsung Semiconductor (San Jose, CA) **May 2023-Aug 2023**

- **Summer Research Internship**
  - Worked as an intern in the memory solution lab (MSL) and researched about software usage and hardware architectures for the future memory / flash technologies.
  - **Manager**: Changho Choi
  - **Mentor**: Jongmin Gim

Publications:

M5: Mastering Page Migration and Memory Management for CXL-based Tiered Memory Systems
Y. Sun, J. Kim, Z. Yu, J. Zhang, S. Chai, M.J. Kim, H. Nam, J. Park, E. Na, Y. Yuan, R. Wang, J.H. Ahn, T. Xu, N.S. Kim.
ACM International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), 2025

Demystifying CXL Memory with Genuine CXL-Ready Systems and Devices
Y. Sun, Y. Yuan, Z. Yu, R. Kuper, C. Song, J. Huang, H. Ji, S. Agarwal, J. Lou, I. Jeong, R. Wang, J. H. Ahn, T. Xu, N. S. Kim.
IEEE/ACM International Symposium on Microarchitecture (**MICRO**), 2023

Making sense of using a SmartNIC to reduce datacenter tax from SLO and TCO perspectives
J. Huang, J. Lou, **Y. Sun**, T. Wang, E. K. Lee, N. S. Kim.
IEEE International Symposium on Workload Characterization (**IISWC**), 2023 **[Best Paper Runner-Up Award]**

Analyzing Energy Efficiency of a Server with a SmartNIC under SLO Constraints
J. Huang, J. Lou, **Y. Sun**, T. Wang, E. K. Lee, N. S. Kim.
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2023

STYX: Exploiting SmartNIC Capability to Reduce Datacenter Memory Tax
H. Ji, M. Mansi*, **Y. Sun***, Y. Yuan, J. Huang, R. Kuper, M. M. Swift, N. S. Kim
USENIX Annual Technical Conference (**ATC**), 2023

RAMBDA: RDMA-driven Acceleration Framework for Memory-intensive us-scale Datacenter Applications
Y. Yuan, J. Huang, **Y. Sun**, T. Wang, J. Nelson, D. Ports, Y. Wang, R. Wang, C. Tai, N. S. Kim
The IEEE International Symposium on High-Performance Computer Architecture (**HPCA**), 2023

Service:

- IEEE Transactions on Parallel and Distributed Systems (TPDS) 2025 – Reviewer

Projects:

RV32IM Processor (Senior Design) **Spring 2021**

- 5-stage pipelined CPU with forwarding
- 2-way pipelined L1d & L1i cache with hardware stride prefetching; 4-way L2; all using BRAM.
- Pipelined Tournament Branch Predictor with 2-bits saturation counter and a block ram BTB. Prediction accuracy > 90% in various workloads.
- 3-cycle 32-bits Wallace-Tree + Modified Booth's Multiplier; 32-cycles divider.
- **Rank #1** in the class out of 25 teams in both speed and power efficiency. 4 times faster than the baseline design while having the same power consumption.

Unix Based OS **Spring 2020**

- Worked in a group of three to design and implement a Unix-based OS.
- The OS has a file system, and supports DMA driven SATA disk write. It also supports multi-terminal with a round-robin scheduler, virtual memory, exceptions, etc.

Django website for picking an easy course **Summer 2020**

- Led a team of four in developing a website for comparing courses with different requirements and rank them by student's comments and average GPA.

- Assigned webpage and database tasks to team members and implement the Django website backbone to connect the pieces together.
- Store the open-sourced data from the university into a MySQL database. Query in the frontend, receive and reply using Django, and use Django to query the MySQL database.
- Deployed the website on cPanel-UIUC with a public domain name.
    - https://easycourseatuiuc.web.illinois.edu

DPI Scholar – AI for Construction, Prof. Mani Golparvar Fard **Spring 2021**

- Worked in a team of 6 to develop a data generation pipeline for deep learning in construction monitoring. The project aims to provide unlimited labeled ground-truth images by generating them synthetically.
- Implemented two ways of generating textured, color-masked, normal and depth images.
    - Wrote a JavaScript extension for Autodesk Forge and collects image in browser.
    - Developed a data generation pipeline with the open-sourced UnrealCV plugin in Unreal 4 gaming engine. This is a more robust method and has generated more than 50GB of synthetic data from construction models.

Technical Skills:

Proficient:

- SystemVerilog, C/C++, Linux Kernel, Python, Java, Golang, x86 and RISC-V asm, R

Intermediate:

- MySQL, MongoDB, Neo4j, Django, Android, JavaScript, Intel SGX